IC Design: Bioinspired Multimoda Signal Perception Enabled System

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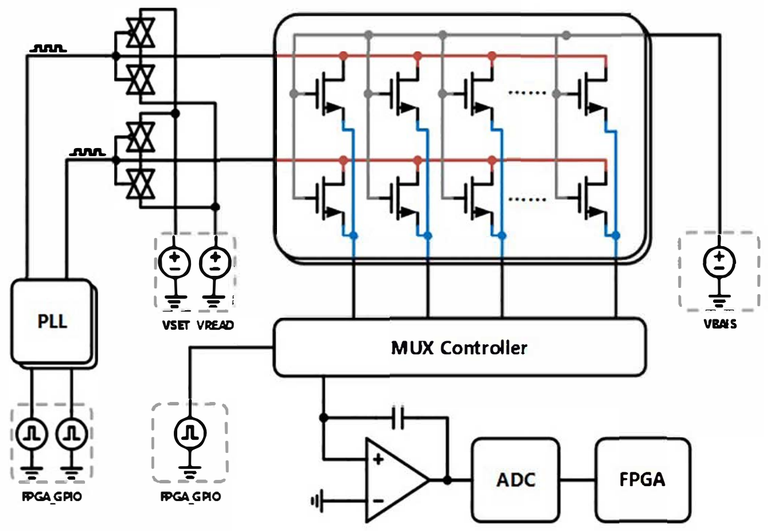
Abstract

Hardware-based Artificial Neural Networks (ANNs) are expected to outperform traditional computers in terms of energy efficiency. This project verifies the feasibility of using a single standard Complementary Metal-Oxide-Semiconductor (CMOS) transistor as an independent artificial synapse unit. Furthermore, it designs an artificial synapse array based on standard CMOS technology and supporting signal processing circuits to explore the feasibility of implementing a complete hardware-based Artificial Neural Network (ANN) architecture in the field of Integrated Circuit (IC) design[1].

Background

The biological brain, with its billions of neurons and synaptic structures, possesses massively parallel data processing capabilities. Despite continuously processing incoming external information, the brain consumes only approximately 20 W of power, making it an ideal reference for ultra-low-power computing.

The research approach of building hardware-based in-memory computing artificial neural network systems to replace traditional von Neumann architecture computers has become one of the mainstream research directions in the semiconductor and microelectronics fields.

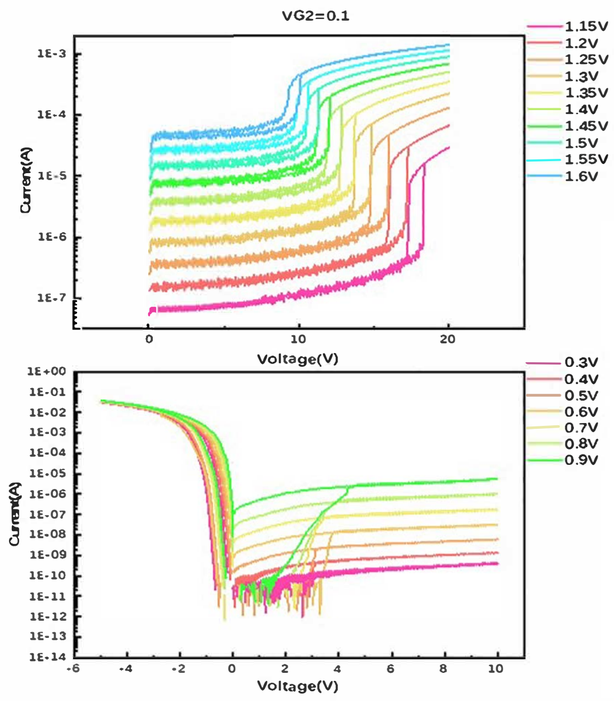


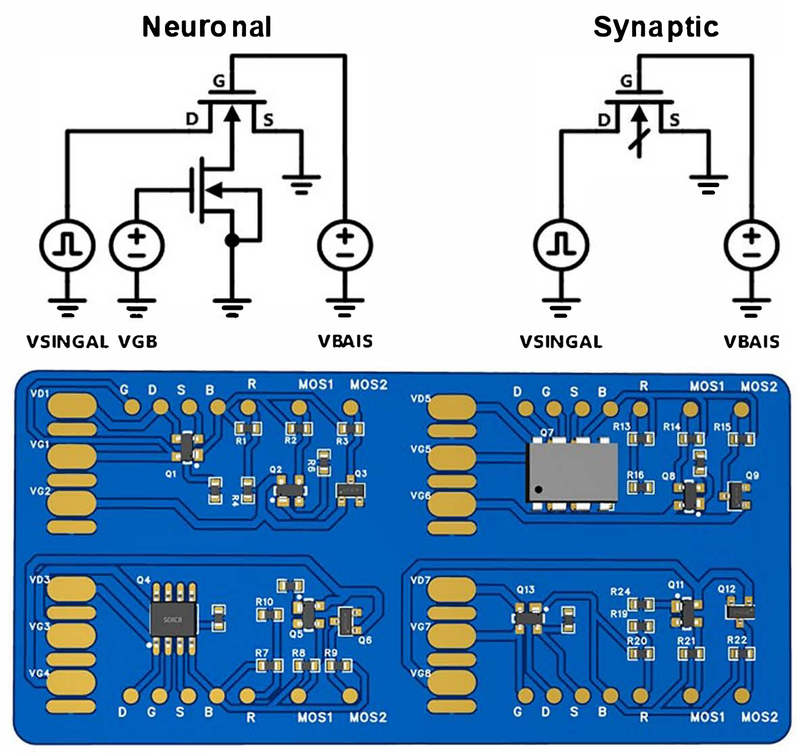
Synaptic device Verification

The artificial synapse array composed of standard Complementary Metal-Oxide-Semiconductor (CMOS) transistors serves as the core for data computation and storage in the system. The approach of computing and storing data in the same location eliminates the energy consumption and latency associated with data transfer.

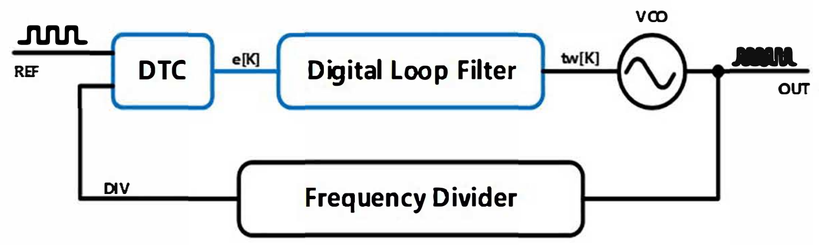
When a voltage is applied to the drain of a CMOS transistor in a floating-body state, hot-hole injection occurs into the dielectric layer of the gate, thereby altering the conductance between the drain and source of the transistor. This enables simultaneous data storage during computation.[1]

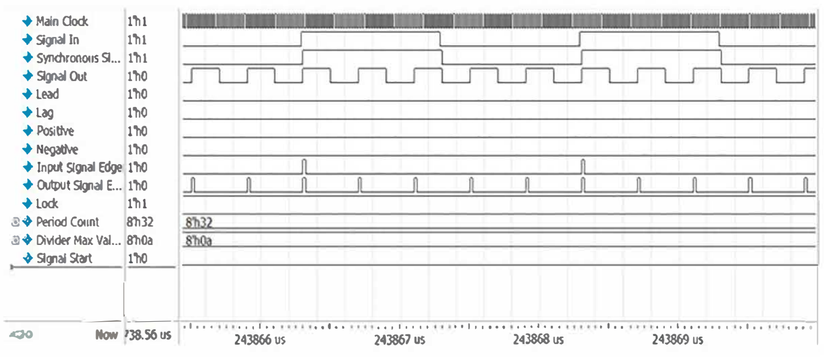
Testing conducted on a designed Printed Circuit Board (PCB) using commercial N-type transistors clearly demonstrates measurable changes in current before and after voltage stimulation.

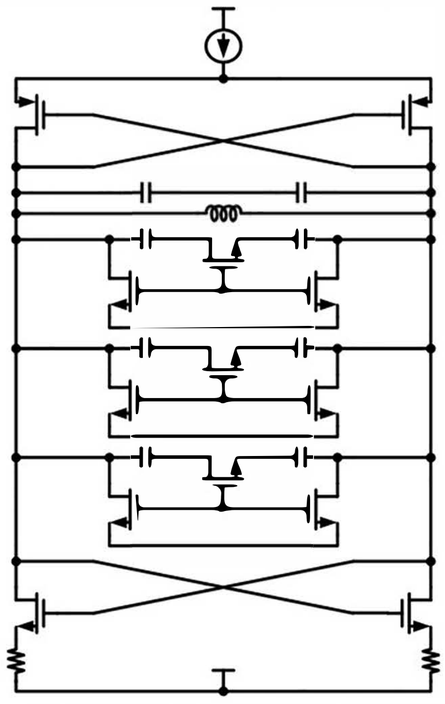




VCO & PLL Circuit







Between the FPGA (Field-Programmable Gate Array) output and the artificial synapse array, a digital PLL (Phase-Locked Loop) regulated by the FPGA is employed to adjust the frequency of the input pulse signals.[2]

By adjusting the value of the parameter DividerMultiple, the frequency divider can modify the frequency multiplication factor of the PLL output, enabling effects such as 2×, 5×, and 20× frequency multiplication based on a 500 kHz input signal.

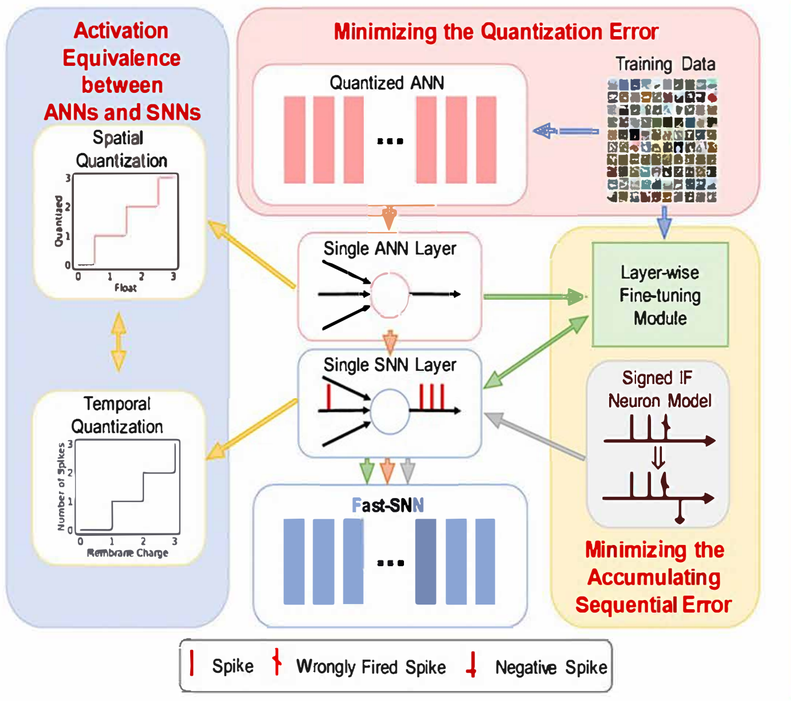
The LC-VCO adjusts the total capacitance of the LC resonator by voltage-controlling the varactor diode's capacitance, thereby precisely tuning the output signal frequency according to the resonant formula. [3]

Verified in the simulator (Cadence Virtuoso), the circuit operates stably with a working frequency of up to 17.59 GHz. At a 1 MHz offset, the phase noise is -101.991 dBc/Hz.

Neuromorphic Application

Spiking Neural Networks (SNNs) deployed on Field-Programmable Gate Arrays (FPGAs) simulate the information processing of neurons in the human brain by switching from high-frequency to low-frequency firing, while filtering irrelevant information and achieving sparse representation.

An activation equivalence-based method was employed to implement the conversion from Artificial Neural Networks (ANNs) to SNNs. Spatial quantization and temporal quantization were applied to process input data, starting with the construction of single-layer ANNs and SNNs, followed by optimization of multi-layer structures using the Fast-SNN method.



Conclusion

This project has developed a neuromorphic computing system based on standard Complementary Metal-Oxide-Semiconductor (CMOS) transistors, which encompasses multiple critical components: feasibility verification of utilizing a single standard CMOS transistor as an independent artificial synapse unit, design of an artificial synaptic array using standard CMOS technology, simulation and implementation of peripheral signal processing circuitry for the array, development of an embedded Field-Programmable Gate Array (FPGA) control module, and the conversion process from Artificial Neural Networks (ANNs) to Spiking Neural Networks (SNNs). Collectively, these efforts systematically validate the feasibility of implementing a standard CMOS-based neuromorphic computing architecture at the system level.

Reference

[1] S. Pazos et al., 'Synaptic and neural behaviours in a standard silicon transistor', Nature, vol. 640, no. 8057, pp. 69–76, Apr. 2025, doi: 10.1038/s41586-025-08742-4.

[2] S. Levantino, "Calibration Techniques in Phased-Locked Loops: Theoretical basis and practical applications," in IEEE Solid-State Circuits Magazine, vol. 16, no. 3, pp. 37-44, Summer 2024, doi: 10.1109/MSSC.2024.3408714.

[3] M. Qu, Y. Li, and Y. Hao, '0.18-μm CMOS process 40 MHz–4.41 GHz frequency synthesizer with high linearity low phase noise varactor-reconstruction LC-VCO', Microelectron. J., vol. 138, p. 105843, Aug. 2023, doi: 10.1016/j.mejo.2023.105843.